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Attestation

Die angehefteten Unterlagen stimmen mit der ursprünglich eingereichten Fassung der auf dem nächsten Blatt bezeichneten europäischen Patentanmeldung überein.

The attached documents are exact copies of the European patent application described on the following page, as originally filed.

Les documents fixés à cette attestation sont conformes à la version initialement déposée de la demande de brevet européen spécifiée à la page suivante.

Patentanmeldung Nr. **Patent application No.** **Demande de brevet n°**

00201166.6

Der Präsident des Europäischen Patentamts;
Im Auftrag

For the President of the European Patent Office

Le Président de l'Office européen des brevets
p.o.

I.L.C. HATTEN-HECKMAN

DEN HAAG, DEN
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LA HAYE, LE

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Blatt 2 der Besch inigung
Sheet 2 of the certificate
Page 2 de l'attestation

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Demandeur(s):
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Titre de l'invention:
Etch stop layer for low epsilon via etching

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Remarques:

Etch stop layer for low epsilon via etching.

The idea describes a method of etching via holes contacting an underlying metal layer of, for example aluminium, copper or tungsten. This metal layer may be covered with a metallic coating such as, for example, titanium nitride (TiN), titanium tungsten (TiW), tungsten nitride (WN) or tantalum nitride (TaN). These metallic coatings are also referred to as capping layers. The above-mentioned vias are etched in a layer of a material of low dielectric constant ('low-k') such as, for example, hydrogen silsesquioxane (HSQ), parylene, a fluorinated polyimide, or "SILK©" which is marketed by Dow Chemical from Midland, Michigan, USA. Metallic polymers are formed when the etching chemistry interacts with the underlying metal (e.g. aluminium, copper or tungsten and/or its metallic coating of e.g. TiN, TiW, WN, TaN). Because these polymers degrade the electrical via resistance much effort has been spent on their removal, which is most efficiently done by 'stripping' them off in a wet chemistry. However, most low-k materials, due to their porous and otherwise unstable nature, appear to be incompatible with this method of wet stripping, that is to say their low-k properties are degraded.

The present invention therefore aims *inter alia* to counteract the formation of these polymers, rather than to remove them. This is realized by applying an etch stop layer between the low-k material and the underlying metal, that is to say a layer with a much lower etch rate than the low-k material itself. For example silicon nitride or silicon carbide appears to be an appropriate choice. In order to make electrical contact the etch stop layer itself has to be etched off in a final step. Because this etch stop layer is very thin and of a well-defined thickness its removal can be done with a well-controlled low power, etch process of short duration. Consequently the interaction with the underlying metal, and thus the formation of metallic polymers is counteracted. Because the etch process has to deal with different types of vias (different in e.g. size, depth, misalignment) the proposed etch stop layer will also improve the margins of the etch process.

The process starts with etching of a metal layer, thereby forming metal structures, for example aluminium structures (figure 1). The top surface of the metal structures comprises a capping layer of, for example, titanium with on top thereof titanium nitride.

Figure1: Metal structures, such as plates, lines and dots, on TEOS

On top of the metal structures an etch stop layer is deposited, which etch stop layer is composed of, for example, silicon carbide (figure 2). Alternatively, the etch stop layer may be deposited on the metal layer prior to the formation of the metal structures. Such etch stop layer is also referred to as selective liner.

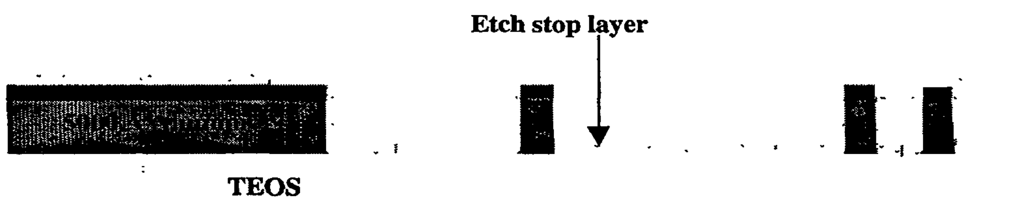

Figure 2: An etch stop layer is deposited on the metal structures.

After the deposition of the etch stop layer, a low-epsilon dielectric such as, for example, hydrogen silsesquioxane (HSQ) is applied to the etch stop layer by means of, for example, spin coating (figure 3).

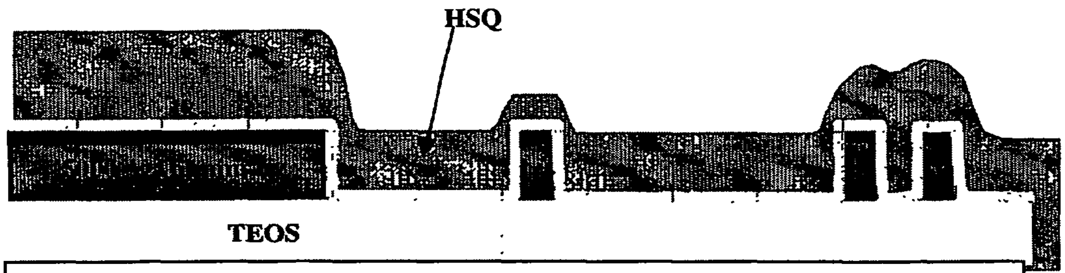

Figure 3: A HSQ layer is spin-coated on the etch stop layer.

Subsequently a TEOS layer is deposited and a chemical-mechanical polishing treatment is performed (figure 4).

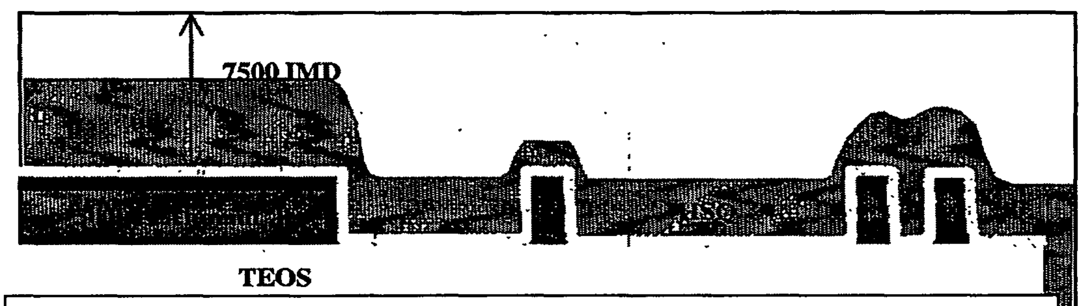

Figure 4: A TEOS layer is deposited and CMPed.

Then, vias are etched through the TEOS layer and the HSQ layer. The etching of these vias stops on the etch stop layer provided on the metal structures (figure 5).

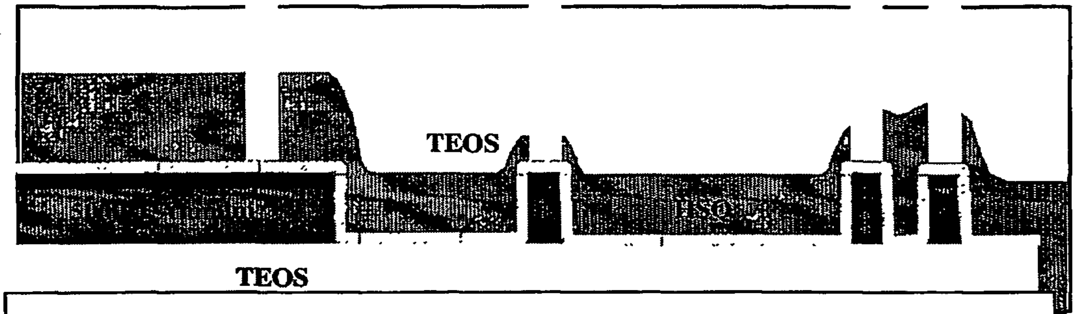

Figure 5: VIAs are etched and land on the etch stop layer.

Next a second etch is performed to remove the exposed etch stop layer within the vias in order to land on the capping layer. Optionally, the exposed capping layer within the vias may be removed as well. In the above way severe polymer formation can be counteracted, as has already been discussed above. The vias are subsequently filled with a conductive material.

The above invention applies to several types of vias, such as a lone via (also referred to as plate via), wherein the via is placed on a big metal plate (see figure 6), a negative overlap via (also referred to as unlanded via), wherein the via is placed on the edge of the metal structure (see figure 7), and a zero overlap via, wherein the via is exactly placed on the metal structure (see figure 8).

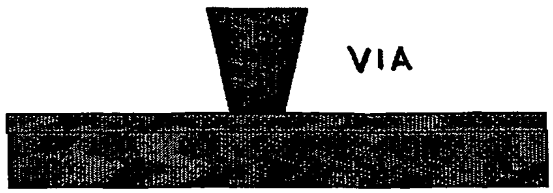

Figure 6

Figure 7

Figure 8

CLAIMS:

1. A method of manufacturing a semiconductor device comprising the steps of:
- providing a semiconductor substrate comprising a conductive interconnect, the conductive interconnect having a top surface portion and side wall portions, of which at least the top surface portion is provided with an etch stop layer,
- applying a dielectric layer,
- etching a via in the dielectric layer over the conductive interconnect, and stopping on the etch stop layer to create an exposed part of the etch stop layer,
- removing the exposed part of the etch stop layer within the via from at least the top surface portion of the conductive interconnect,
- filling the via with a conductive material
characterized in that
a layer comprising silicon carbide is applied as the etch stop layer.

2. A method as claimed in claim 1, characterized in that the step of providing a semiconductor substrate comprises providing the semiconductor substrate comprising the conductive interconnect, and applying the etch stop layer to the top surface portion and the side wall portions of the conductive interconnect.

3. A method as claimed in claim 2, characterized in that the step of etching a via comprises etching the via, the via overhanging at least one of the side wall portions of the conductive interconnect and exposing at least part of the etch stop layer covering the top surface portion and the at least one of the side wall portions of the conductive interconnect.

4. A method as claimed in claim 3, characterized in that the step of removing the exposed part of the etch stop layer comprises removing the etch stop layer within the via from only the top surface portion of the conductive interconnect.

5. A method as claimed in claim 2, 3 or 4, characterized in that the step of applying an etch stop layer comprises applying the etch stop layer to the entire semiconductor substrate.

6. A method as claimed in any one of the preceding claims, characterized in that the step of providing a semiconductor substrate comprises providing the semiconductor substrate wherein the conductive interconnect is comprised at least in part of a material selected from a group comprising aluminium, copper and tungsten.

7. A method as claimed in any one of the preceding claims, characterized in that the step of providing a semiconductor substrate comprises providing the semiconductor substrate wherein the conductive interconnect comprises a capping layer providing the top surface portion of the conductive interconnect.

8. A method as claimed in claim 7, characterized in that the method further comprises the step of removing the capping layer within the via prior to filling the via.

9. A method as claimed in claim 7 or 8, characterized in that the step of providing a semiconductor substrate comprises providing the semiconductor substrate wherein the capping layer is comprised of a material selected from a group comprising titanium nitride, titanium tungsten, tungsten nitride and tantalum nitride.

10. A method as claimed in any one of the preceding claims, characterized in that the step of applying a dielectric layer comprises depositing a dielectric material having a dielectric constant lower than that of silicon oxide.

11. A method as claimed in claim 10, characterized in that the step of applying a dielectric layer comprises depositing a material selected from a group comprising hydrogen silsesquioxane, parylene and a fluorinated polyimide.

12. A method as claimed in any one of the preceding claims, characterized in that the step of filling the via comprises depositing a layer comprising a metal selected from a group comprising aluminium, copper and tungsten.

13. A method as claimed in claim 12, characterized in that the step of filling the via comprises depositing a double-layer consisting of a first sub-layer acting as adhesion layer and/or barrier layer with on top thereof a second sub-layer comprising the metal.